Attend the Technology Seminar: 
ASIC Prototyping with Xilinx’s Virtex UltraScale 440 Platform

Hosted by

S2C invites you to join a half-day seminar on using Virtex UltraScale 440 to solve prototyping challenges caused by growing SoC design size and increasing performance demands.

Who Should Attend:
SoC prototyping engineers
SoC emulation engineers
ASIC project managers
ASIC designers

Why You Should Attend:
ASIC prototyping teams can expect twice as many logic cells and block RAMs on a single FPGA reaching up to 44M ASIC gates in Xilinx’s Virtex UltraScale 440 FPGA. The increase in capacity will also be met with significant performance enhancements including faster speed performance and integration with up to a 50% reduction in power consumption, 30% improvements to transceiver bandwidth, a 2400 Mb/s DDR4 interface, and integrated endpoint blocks for PCIe Gen3.

S2C’s VU440 prototyping platform family, using Xilinx’s Virtex UltraScale 440 FPGA, will be able to leverage joint Xilinx and S2C technologies for users to prototype their latest large designs.

Event schedule and venue:

Seminar date: September 4, 2015 (Friday)
Seminar time: 13:30 ~ 17:30
Location: 新竹科學園區科技生活館(2F) 愛迪生廳
Address: 新竹市科學園區工業東二路1號, 電話 (03) 577-9191

Seminar agenda:

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<th>Time (PM)</th>
<th>Subject</th>
<th>Speaker</th>
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<tr>
<td>1:30-2:00</td>
<td>Reception</td>
<td>Jimmy Chen</td>
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<td>2:00-2:10</td>
<td>Welcome – A new era for FPGA Prototyping</td>
<td>Cliff Tsai (Xilinx)</td>
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<td>2:10-2:30</td>
<td>The leading Xilinx technology roadmap and update</td>
<td>Elliott Wu (ANStek)</td>
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<td>2:30-3:00</td>
<td>UltraScale Architecture &amp; new features for ASIC prototyping</td>
<td>Sherman Hung</td>
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<td>3:00-3:30</td>
<td>Solving Prototyping Challenges with S2C’s VU440 platform offerings</td>
<td>Rex Liu</td>
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<td>3:30-3:50</td>
<td>Tea Break</td>
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<td>3:50-4:20</td>
<td>Live demos: experience S2C’s VU440 features with</td>
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<td>· High-speed interfaces using GTH, Single-ended or LVDS</td>
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<td>· Implementing your DDR4/DDR3 memory and debugging</td>
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<td>· Prototyping large design with multiple systems using LVDS</td>
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<td>4:20-5:00</td>
<td>Addressing Vivado Timing Challenges for VU440</td>
<td>Elliott Wu (ANStek)</td>
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<td>· Baseline Constraints</td>
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<td>· Timing Closure Techniques</td>
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<td>5:00-5:20</td>
<td>Panel discussion</td>
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Seminar registration:
Please copy the following registration form and email your user information to Sherman Hung at S2C from your company email account. Seats are limited, S2C will confirm your registration on a first come first serve basis.

Sales manager: Sherman Hung, Email: shermang@sin.com
Office phone: +886-3-667-5782 Ext 210, Mobile: +886-932-386-248

報名表

| 公司名称 | | |
|---|---|
| 姓名 | | |
| 電話 | | |

Speaker Profiles:
Cliff Tsai, Distribution Sales Manager of Xilinx Taiwan
Cliff has 10 years of FAE and technical management experience at Xilinx Taiwan. Now he is responsible for Distribution FAE management and Marketing activities in Taiwan.

Elliott Wu, Xilinx FAE Manager, ANStek
Elliott has been in FPGA industry for 12 years, and specializes on high speed design. Elliott is in charge of FAE team in ANStek to support key ASIC prototyping accounts in Taiwan.

Jimmy Chen, VP of Product Solution Sales at S2C
Jimmy has been promoting ASIC prototyping methodology since joining Synplicity in year 2000 as the sales director of Asia. Jimmy started as an IC design engineer 25 years ago.

Sherman Hung, Sales Manager of S2C Taiwan
Sherman has been in the ASIC prototyping industry for 15 years, and was an FAE with Synplicity focusing on ASIC prototyping applications.

Rex Liu, FAE of S2C Taiwan
Rex has 10 years of experience in ASIC testing beginning with his work at Compal. Rex is an expert on network applications.