



White Paper

Exercising H.264 Video Compression Using Commercial FPGA Prototypes

S2C Inc.

1754 Technology Drive, Suite 620

San Jose, CA 95110, USA

Tel: +1 408 213 8818

Fax: +1 408 549 9948

www.s2cinc.com

1. Introduction

The H.264/Advanced Video Coding (AVC) video compression standard achieves the best-ever compression efficiency for a broad range of applications. It can produce excellent video quality from 3G to HD and everything in between.

The implementation of H.264 is very complicated, so most designers prefer to choose sophisticated, verified H.264 intellectual property (IP) rather than developing it themselves, to shorten the lead time to market and significantly reduce their risk. However, selecting an appropriate commercial IP core, such as an H.264 encoder IP core, is not straight-forward. Project managers must balance a variety of factors—such as features, performance, die size, power consumption, maturity, price, support and roadmap—to decide on the best possible core for their project. Unfortunately, many of these decision factors are difficult to determine before the IP is actually licensed.

In response, silicon IP vendors are increasingly utilizing FPGA prototypes as the vehicles for both pre-sales and post-sales support of their IP cores.

With FPGA prototypes, IP vendors can let potential customers see and evaluate an IP core securely, at near real-time speed. The FPGA prototype also can serve as a reference design for customers to speed up their design process after the IP licensing transaction is complete.

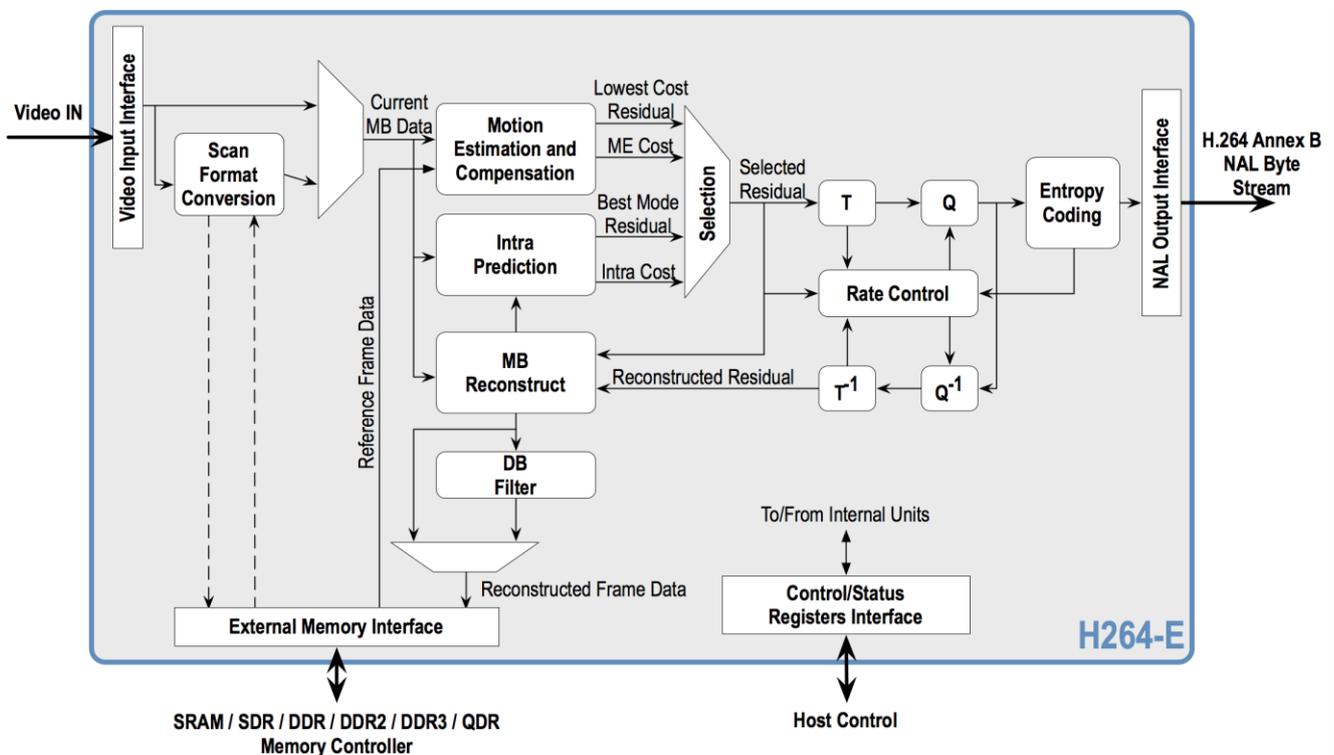
A number of firms already offer FPGA-based reference boards for IP evaluations, but these are usually very primitive and not suitable for designers to test IP cores with other designs or to build system prototypes. To address this challenge and meet both needs, S2C provides a commercial FPGA prototyping tool, TAI Logic Module and related software applications that can serve as a common and scalable FPGA-based system prototyping platform.

This paper describes how S2C's partner CAST, Inc. has used S2C's TAI Logic Module to build an H.264 Encoder Reference Design System, which enables customers to evaluate video compression at near real time and to integrate IP to form complete system prototypes. The paper describes the components and approach as well as the key advantages of using S2C's TAI Logic Module as the platform to promote and support IP cores.

2. The H.264 Encoder IP core

Alma Technologies S.A. offers its innovative H.264 Encoder core via its marketing and sales partner, CAST. The core implements a video encoder in hardware that uses the Baseline profile of the H.264 Advanced Video Coding (AVC) standard (up to level 5.1), also known as MPEG-4 Part 10. It receives video frames, outputs the H.264 encoded bit-stream, and saves decoded reference frames to an external memory. The H.264 core can process up to 1080p HDTV video.

Figure 1: Block Diagram of the H.264 Encoder IP Core



The efficient encoder requires minimal host intervention: it only needs to be programmed once with the encoding options, and it can then encode an arbitrary number of video frames. The core's simple and flexible external memory interface makes it independent of memory type—supporting SRAM, SDRAM, or DDRAM—and tolerant to the large delays and latencies typically present on a shared bus architecture. The core is designed for reuse and reliability, and has been rigorously verified.

Developed for easy integration, the H264-E includes a complete verification environment plus additional aids for system-on-chip simulation, such as a software bit-accurate model (BAM). It is suitable for a wide range of video rates and applications, including surveillance and monitoring, video conferencing, video-on-demand and other SD and HD Video applications. Following are the H.264

encoder core's main features.

- Fully compliant to the ISO/IEC 14496-10/ITU-T H.264 baseline specification (MPEG-4 Part 10)
- Profile level up to 5.1
- Flexible 4:2:0 YCbCr digital video input
- Planar scan
- Interleaved scan
- Macroblock scan
- ITU-T H.264 Annex B compliant NAL byte stream output
- HRD compliant CBR NAL output
- No host CPU assisted, standalone operation
- Compression efficiency from QCIF up to HD resolutions
- Sub-frame, accurate rate controlled encoding mode
- CQP- VBR encoding mode
- Full search, variable block size, sub-pixel motion estimation engine
- Sophisticated block skipping logic
- Advanced Intra prediction
- Advanced Intra prediction in Inter slices
- Multiple slices for enhanced error resilience
- Optional advanced thresholding of quantized transform coefficients
- Run-time tunable operation enables decoder compatibility trade offs
- Simple, microcontroller like, programming interface
- Registered I/O ports
- High speed, flow controllable, streaming I/O data interfaces
- Low video latency
- Low requirements in external memory bandwidth
- Flexible external memory interface
- Independent of external memory type
- Tolerant to latencies
- Allows for shared memory access
- Can operate on independent clock domain
- Optional deblocking Filter
- Bit Accurate Model
- Test Vector generation

3. CAST H.264 Encoder Reference Design on S2C Virtex-5 TAI Logic Module

The H.264 encoder reference design is built on S2C's TAI Logic Module. The H264-E encoder core and the necessary system and memory interface cores are all implemented in a Xilinx Virtex-5 FPGA on a S2C Single 5V330 TAI Logic Module. The details for each core and how they are implemented on the S2C V5 TAI Logic Module are described below.

H264-E H.264/AVS Baseline Video Encoder Core

This encoder core consumes about 20,000 slices for 1080p video at 30 frames per second (fps). It consists of purely digital logic, and consumed about (38%) of the logic resources in a Xilinx Virtex-5 330LX FPGA.

DDR2-SDRAM-CTRL SDRAM Memory Controller Core

This controller core works with the H.264 encoder, reading from and writing to the DDR2 memory installed directly on a V5 TAI Logic Module DDR2 SO-DIMM socket. The V5 TAI Logic Modules' two on-board DDR2 SO-DIMM sockets can support DDR memory of up to a 533Mbit data rate.

CPXP-EP PCI Express Endpoint Controller Core

This x1 PCIe core handles communication to and from a host PC or laptop system with a single lane (four (x4) and eight (x8) lane versions handle greater bandwidth). S2C provides an x1 PCI-e PHY Interface Module, enabling user designs in TAI Logic Modules to interface to one-lane PCI Express v1.1 devices through TI's XIO1100 PHY chips. It connects to the host PC through PCIe PC cards and a cable from one-stop-system.

CMMI-H264-E CAST Multimedia Interface for H.264 Core

Implements a simple interface between the AMBA™ AHB bus and the H264-E core. It integrates data paths for core control register access, stream data transfer in both directions, and a dual-channel DMA controller. The CMMI-H264-E allows removing stream-in or stream-out data paths.

The H.264 and DDR2 cores were developed by Alma Technologies, the PCIe and MMI by CAST, and the reference design integration and board was a joint effort of CAST, Alma Technologies, and S2C.

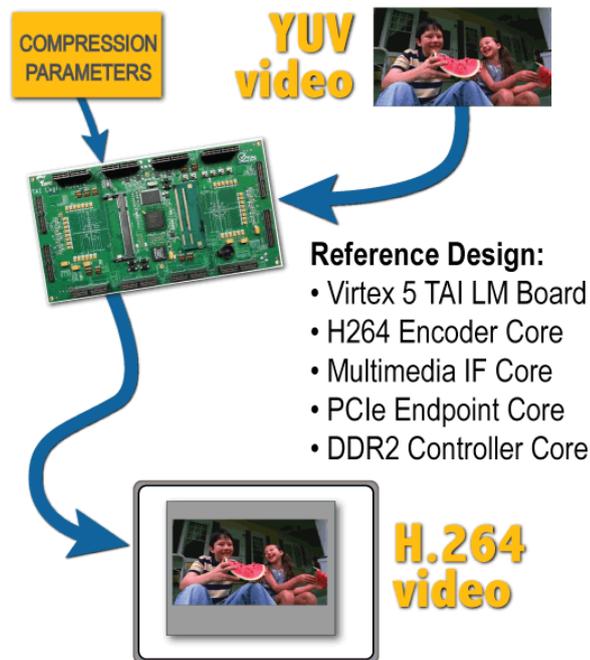
The table below shows the resources consumed by the Reference Design in a Virtex-5 FPGA.

Table 1: H.264 encoder reference design resource consumed in a Xilinx FPGA

Xilinx Devices	Slices	BRAM	Special Features	Resolution
Virtex-5	24,000	46	39 DSP48; 2 DCM	1080p @ 30fps

The Reference Design System reads a video file in standard YUV format provided by the host system via a graphical user interface. A designer can set various compression parameters to configure the IP core to achieve different features and experiment with compression/quality trade offs. It then produces H.264 video, which is sent back to the host system for streaming display or file storage via the PCIe connection. The figure below shows the data flow of the Reference Design.

Figure 2: Data flow of the H.264 Reference Design System



The next figure is an actual photo of the system set up, which is comprised of one S2C Single 5V330 TAI Logic Module, one PCI express interface card, one DDR2 SDRAM, and one configuration flash. The PCI express interface connects the demo board with PC, whereby PC can interface the demo board for transferring files or configurations. The DDR2 SDRAM is used for the processing for H.264 encoder and the configuration flash is used to program the FPGA in board.

Figure 3: Photo of the H.264 Reference Design System on S2C's TAI Logic Module

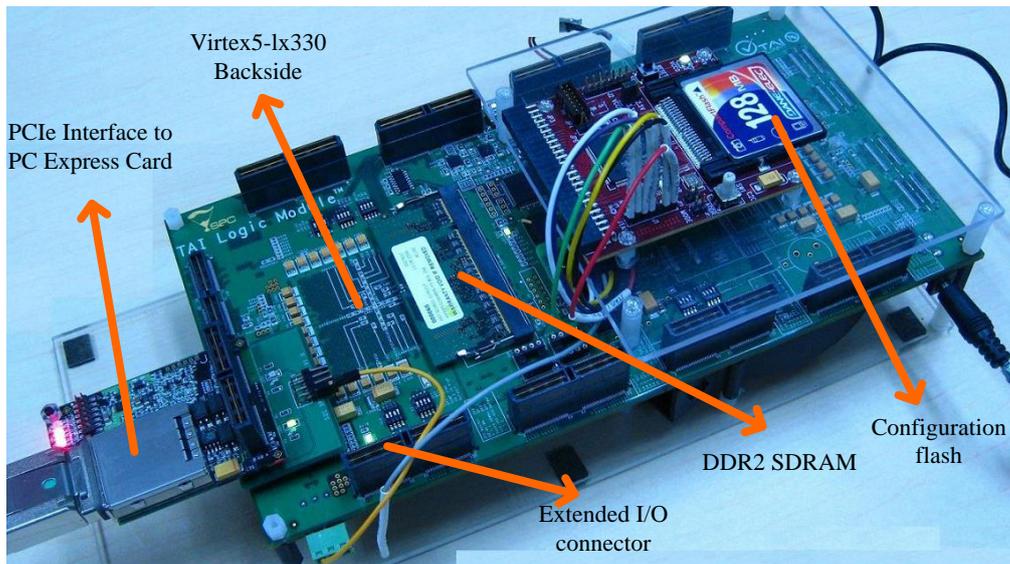
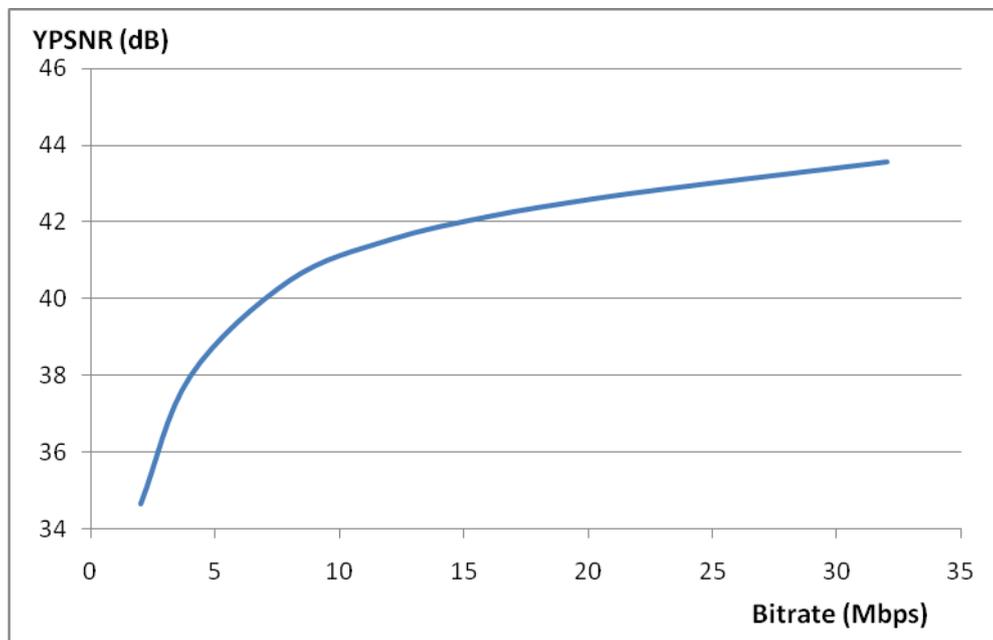


Figure 4 provides rate-distortion data acquired using the reference design on the TAI Logic Module to encode the “pedestrian area” 1080p@30fps clip.

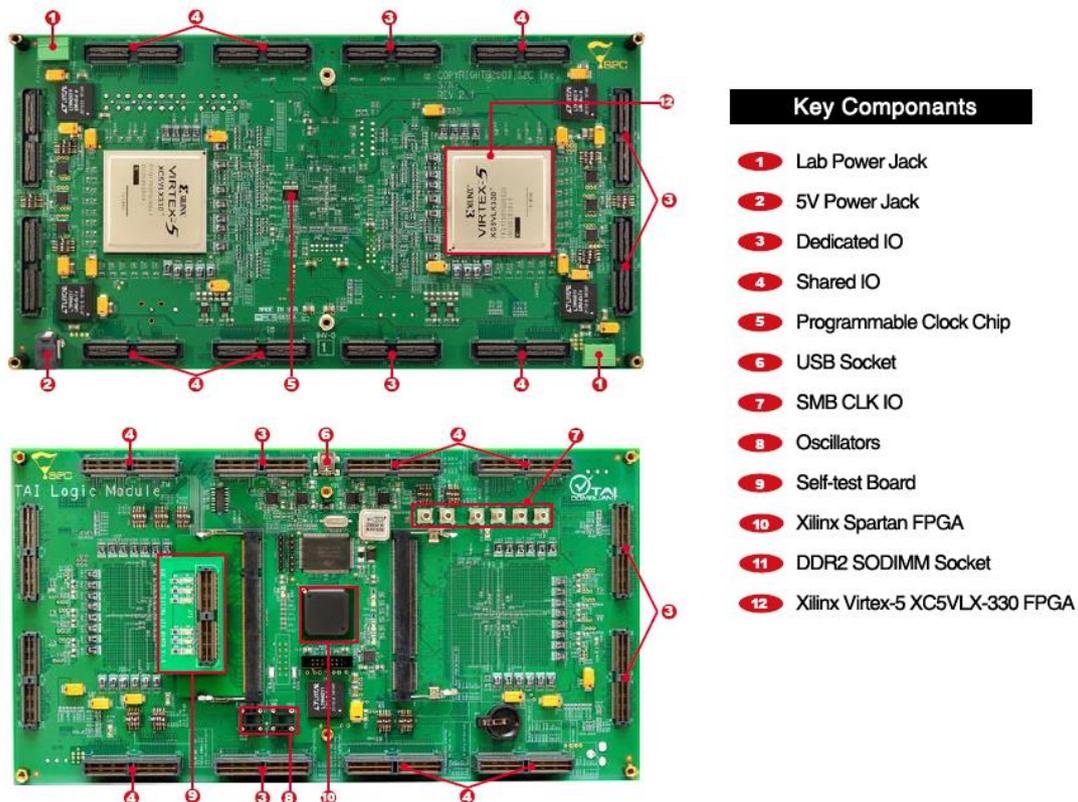
Figure 4: Rate – Distortion of HD1080



4. Benefits of the TAI Logic Module for H.264 Prototyping

S2C's mission is to provide FPGA-based electronic system level (ESL) solutions that allow designers to easily and securely employ commercial silicon IP to quickly assemble system prototypes with FPGAs and immediately start software development. Accordingly, S2C TAI Logic Modules are designed to provide secure IP evaluation and easy IP integration. The key features of the S2C Virtex-5 TAI Logic Module used to build the CAST H.264 Reference design are listed below:

- ✓ 6.6 million ASIC gates on one S2C 5V TAI Logic Module (stackable for designs that require even larger capacity)
- ✓ Two DDR2 SO-DIMM sockets supporting 4GB of memory at up to 533MHz
- ✓ Large library of off-the-shelf daughter boards such as ARM interface, PCIe, Gigabit Ethernet PHY, and various types of memories
- ✓ In command of FPGA prototypes from PC software through USB
- ✓ TAI Player Pro application software that supports design partition, pin-assignment, probe insertion and multi-FPGA internal logic analyzer (ILA)



By using the S2C TAI Logic Module with its associated daughter boards and software applications, designers who are interested in H.264 video encoding can enjoy the following benefits

- ✓ Execution of the hardware H.246 Encoder Core on a designer's own video material, an

easier and more effective practice than judging video compression quality from datasheets or even simulation models.

- ✓ Secure H.264-E IP evaluation together with other designs on FPGA prototypes (requires the use of a Dual 5V330 TAI Logic Module).
- ✓ Rapid system prototyping of designs with H.264-E IP after the IP is licensed: CAST offers the entire Reference Design System including the TAI Logic Module.

5. Conclusions

Semiconductor IP cores are the building blocks for today's SoCs, and they often determine the success or failure of an SoC project. Adopting IP cores that have been validated on commercial FPGA prototypes can effectively reduce the risk of licensing the IP for a SoC project. CAST has chosen S2C's TAI Logic Module to build its H.264 Encoder demonstration platform, enabling customers to evaluate IP cores easily at near real-time, and to integrate IP to form complete system prototypes rapidly after the IP is licensed. S2C's TAI Logic Module thus helps designers enjoy greater peace of mind when licensing IP from CAST.

Learn more:

- S2C, Inc. — www.s2cinc.com
- Alma Technologies S.A. — www.alma-tech.com
- CAST Inc, — www.cast-inc.com