FPGA PROTOTYPING SOLUTIONS

Success Story

Inspur

Overview

- S2C's single VU440 Prodigy Logic Module providing multi-million ASIC gate capacity
- The Prodigy Multi-Debug Module (MDM) enables greater sampling depth which makes debugging easier
- The customized QSFP Interface Module is well designed and higher performance
- The quick response of S2C's support team helped Inspur to bring up the FPGA validation environment successfully

Within S2C's rapid SoC prototyping solutions, Inspur saved about six months in developing and debugging their SoC design. Features like scalability, reuse, flexibility, and deep trace debugging let Inspur quickly port the design into FPGA prototyping, transfer mass packet to the DUT, and speed up the debugging progress.

About Inspur

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As a leading total solution and service provider of cloud computing, Inspur is capable of providing total solution at IaaS, PaaS and SaaS levels. With high-end servers, mass storages, and cloud operating system and information security technology, Inspur offers advanced cloud computing infrastructure platform for its customers. Based on Inspur's information software for government, enterprise and industry, as well as terminal products and solutions, this platform provides comprehensive support to the construction of smart government, and enterprise cloud and vertical industry cloud.

Challenges

- Establish an executable platform for hardware validation and integration
- Build a high bandwidth transmission channel to transfer mass packet to DUT for verification
- Support fast and stable system startup then quickly and accurately locate problems

S2C Solution

- S2C's Single VU440 Prodigy Logic Module providing multi-million ASIC gate capacity allows Inspur to quickly port their routing control chip for verification
- Customized two QSFP cage interface modules to provide the high-speed transmission channel for the DUT
- Specialized Prodigy Multi-Debug Module hardware enables deep trace debugging with the ability to store up to 16GB of waveforms
- Prodigy Player Pro is used to setup trigger conditions and capture related packets for chip-level debugging

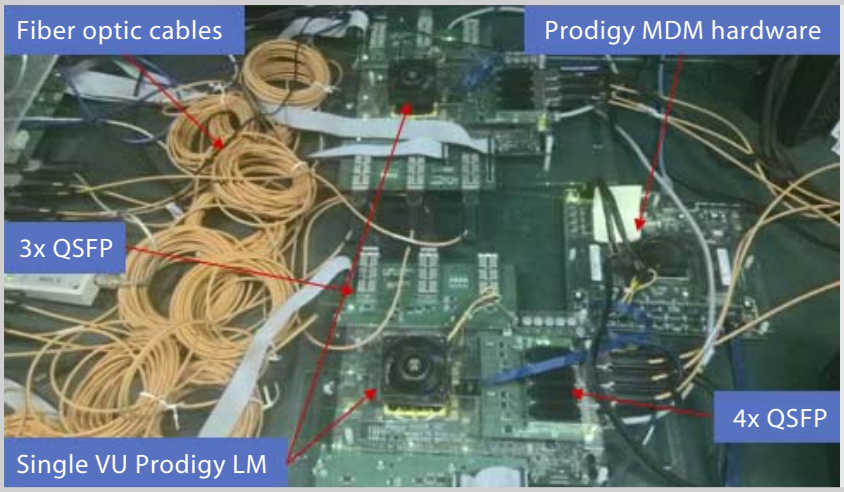

Figure 1:
Inspur routing controller validation platform using S2C Single VU440 + MDM

Implementation Details

Inspur's routing control design consumed 96% BRAM of VU440 FPGA which allowed no extra memory resources for ChipScope debugging. The S2C delivered MDM does not consume design FPGA memories which perfectly solved this debugging issue.

The complexity of Inspur's SoC increased both cost and schedule risks due to the need to verify real-world scenarios. Generally no one knows when a bug happens or when it occurs especially if there isn't enough sampling depth to analyze. MDM mitigated those challenges as a cost-effective solution. After the initial 1~2 MDM and Single VU systems bring up, Inspur used 10 sets of systems running 24 hours a day without interruption. This enabled Inspur to detect and fix many bugs in the real network testing environment which cut six months off their development schedule.

Results

Inspur used the Single VU440 Prodigy Logic Module for prototyping verification on a routing control chip, the design consists of mass packet transmissions. And selected the MDM to run the deep trace debugging, the Prodigy MDM is also used to set trigger conditions and capture related packets for chip debug. The deep sampling depth allows Inspur to grab as many packets as possible to then be analyzed for correctness. All these helped Inspur efficiently verify the routing control SoC design met the specification and reduce the total engineering cost and project effort.

"The performance capabilities of the Prodigy Logic Module, deep trace debugging of MDM software, professional daughter card customization services, and fast support helped us efficiently verify our SoC designs. This allowed us to focus on the innovation and validation of the SoC."

"The biggest advantage S2C MDM gives us is the ability to detect bugs deeply embedded in the design that can be detected only by processing the real word packets. This significantly speeds up the debug process and gets our design to the market quickly with greater confidence."

Huang Jiaming
General Manager of High-end Server Department