

# Trinity

## Multi-Format High Definition Video Decoder IP

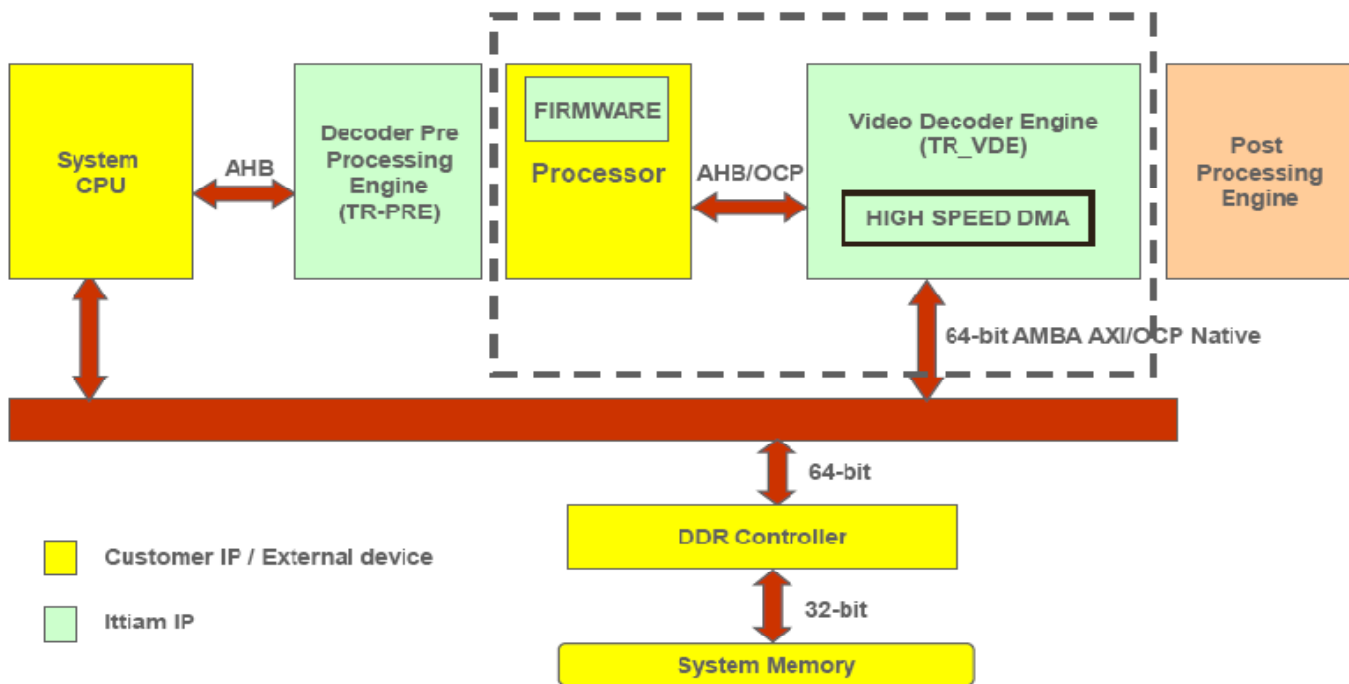
### Overview

Ittiam's Multi-format High Definition Decoder is a fully synchronous, single clocked design, with special optimization techniques applied for low power dissipation.

The Decoder Core supports a wide range of common video formats, including H.264 upto High Profile, VC1 Advanced Profile, MPEG-4 Advanced Simple Profile, MPEG-2 and MPEG-1 Main Profile at High Level, DivX 4/5/6, AVS Jizhun Profile, RMVB 8/9/10, H.263 Base Profile and JPEG at resolutions of 1080i. The Multi-Format Video Decoder Core can also support multiple streams of High Definition and Standard Definition decodes.

Apart from verification in an ASIC design environment, Ittiam's Multi-Format High Definition Video Decoder Core is also verified on Ittiam's MFHDVDEC Validation Platform, which includes Ittiam's Video Decoder Core and a DDR controller synthesized to an FPGA, an ARM9E based controller device, Hard Disk Storage, USB and HDMI interfaces. The Platform is capable of executing real time decodes at 1080i, allowing for more detailed verification of Ittiam's IP Core.

### Block Diagram



## Supported Formats

- H.264 upto High profile (HP @ L4.1)
- VC1 Advanced Profile @ L3 with Main Profile
- MPEG-2 and MPEG-1 Main Profile at High Level
- MPEG-4 Advanced Simple Profile
- H.263 Base Profile Standard
- HD JPEG imaging standard
- DivX 4/5/6
- AVS Jizhun Profile
- RMVB 8/9/10

## Features

- Input: Encoded Video Elementary Streams or Mux'ed Transport Streams
- Output: Decoded streams in YUV 422 format
- Direct Interface to Transport streams from digital tuners
- AXI™ compliant for the memory interface
- AHB™ compliant interface for host CPU
- Supports video resolution at 1080i/1080p @ 30 fps @ 90nm Process
- Supports multiple stream decoding for High definition and Standard definition
- Supports High Speed DMA
- Bandwidth optimized access to external DDR via 32-bit memory interface
- Error Resilience
- De-blocking Filters for MPEG-2 & MPEG-4 (H.264 & VC1 –In-loop ; MPEG-2 & MPEG-4 - out of loop)

## Validation Platform

- FPGA based platform
- Hard Disc Drive interface for loading input streams
- Built-in DDR Controller on FPGA for DDR access
- USB interface for PC download of streams
- HDMI Interface for direct display on HDTV
- ARM9 based Control and Audio Processors on board
- Decode of 1080i HD on board

## Target Applications

- High Definition DVD Players
- High Definition Set Top boxes
- IPTV Solutions

## Deliverables

- Multi-format HD Decoder IP RTL (Verilog)
- Firmware as ANSI C code
- Test Plan and Test Reports
- User Guide & Documentation
- Synthesis Scripts

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