

Dual Virtex-4 TAI Prototyping Development Kit

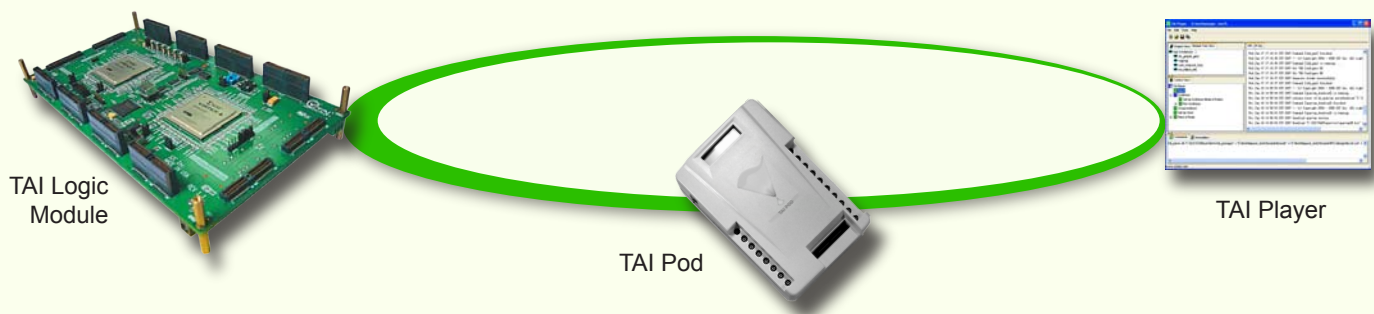
TAI Logic Module + TAI Pod + TAI Player



Overview

The Dual Virtex-4 TAI Prototyping Development Kit (TAI PDK) is an integrated FPGA-based prototype design suite that enables IC designers to easily construct efficient SoC prototypes in a cost-effective manner. The design kit is comprised of three flagship S2C products - Dual Virtex-4 TAI Logic Module prototyping board, TAI Pod prototype-to-PC hardware interface, and TAI Player design flow automation software.

TAI PDK comes in two logic capacity levels: the TAI-PDK-4V200D offering 4 million logic capacity gates (two Xilinx Virtex-4 LX200 FPGAs) and the TAI-PDK-4V160D offering 3.2 million logic capacity gates (two Xilinx Virtex-4 LX160 FPGAs).



Prototyping Hardware Features

- Capacity: up to 4 million ASIC gates with two Xilinx Virtex-4 LX200 FPGAs
up to 3.2 million ASIC gates with two Xilinx Virtex-4 LX160 FPGAs
- Performance: 500 MHz clocking in single FPGA, 400 MHz differential FPGA to FPGA
- 32 global clocks
- 480 dedicated external I/Os
- 624 inter-FPGA connections, can be used as external I/O

Compile Features

- Compile Verilog / VHDL
- Support bottom-up and incremental synthesis using XST and Synplify/Synplify Pro
- Group IP (design modules) into different FPGA automatically or through instance groups, flattening hierarchy features to guide FPGA grouping
- Automatically handle internally generated clocks and asynchronous reset
- Assign I/Os and their properties in GUI, avoiding errors

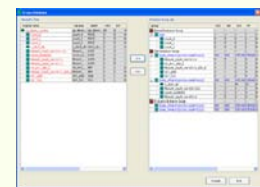
Runtime Features

- Fast and easy FPGA download from PC
- Advanced clock generation
 - 4 configurable base clocks from 1 MHz to 200 MHz
 - 16 phase-adjustable synchronized clocks generated from 4 base clocks
 - 2 OSC sockets
 - 6 SMB clock inputs
 - 24 clock feedback lines
- Comprehensive hardware self-test

Enhanced productivity with bundled TAI Player software



RTL Probing



Automatic IP Grouping



Advanced Clock Generation

S2C Inc. Powering FPGA-Based ESL

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