Whitepaper

FPGA Prototyping in Practice: Addressing Peripheral Connectivity Challenges

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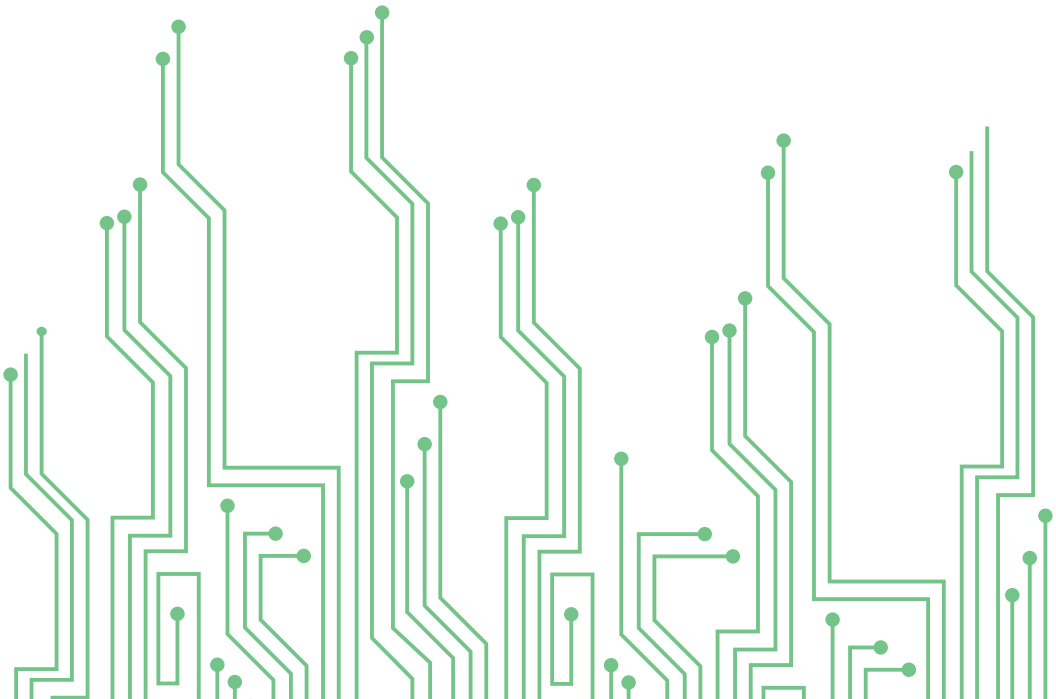


Modern chip design verification often encounters challenges when connecting peripherals, primarily due to drastic differences in operating speed or hardware limitations. Designs running on hardware emulators or FPGA prototyping platforms typically operate at clock frequencies of tens of megahertz, and in some cases even below one megahertz. In contrast, real-world peripherals and protocols, such as PCIe and high-speed Ethernet, operate at hundreds of megahertz or higher. This significant gap in operating speed makes direct connections between the prototype and peripherals almost impossible.

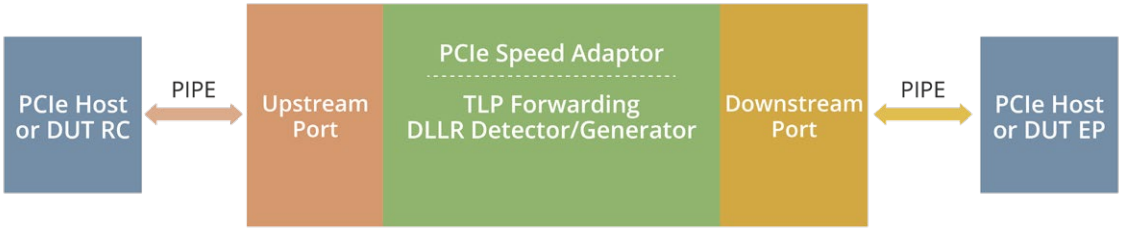
To address speed mismatches, a common and effective solution is the use of a speed adaptor. A speed adaptor is a specialized hardware interface used in prototyping or emulation environments. Its primary function is to bridge systems that operate at very different speeds. This enables verification leveraging real-world transactions rather than pure models. In situations where the hardware does not support a particular peripheral or interface, functional and protocol behavior can be emulated using models and interface IP.

Three typical application cases illustrate the practical use of speed adaptors and memory models in FPGA prototyping:

Case 1: PCIe Speed Adaptor

Speed adaptors address several key challenges, including speed adaptation, protocol conversion, time decoupling, and providing controllability and observability for debugging purposes. In FPGA prototyping, the working frequency of AMD (Xilinx) PCIe PHYs ranges from 62.5 MHz for Gen1 to 500 MHz for Gen4, which is far higher than the operating frequency of synthesized user designs. When a user design is partitioned across multiple FPGA boards, the effective operating frequency can drop below 20 MHz. This creates a substantial mismatch with the PCIe PHY frequency, making reliable speed adaptation critical.

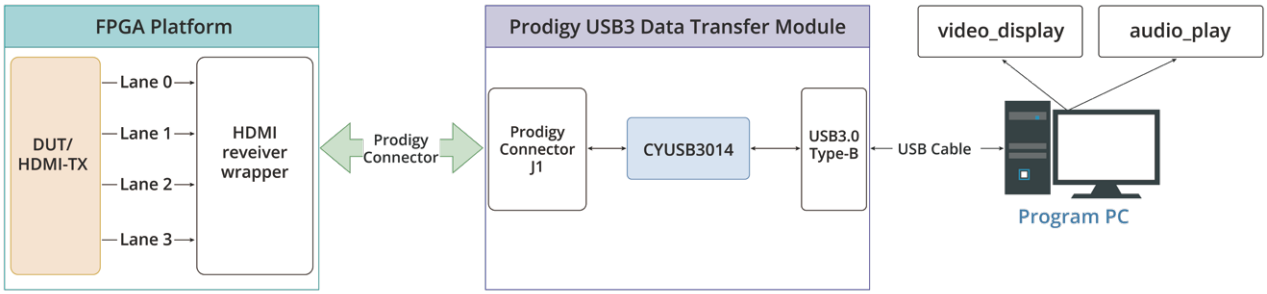
The core solution for PCIe speed adaptation is the PCIe Switch IP. Its multi-port architecture allows independent link establishment and operation in different states. This enables dynamic adaptation of protocol versions, link width, and speed. The solution also integrates essential IP blocks for PCS and PIPE interface conversion, forming a complete approach for speed adaptation in PCIe systems. With this architecture, FPGA prototypes can interface with high-speed PCIe devices while maintaining functional correctness and reliable communication.



Case 2: HDMI Speed Adaptor

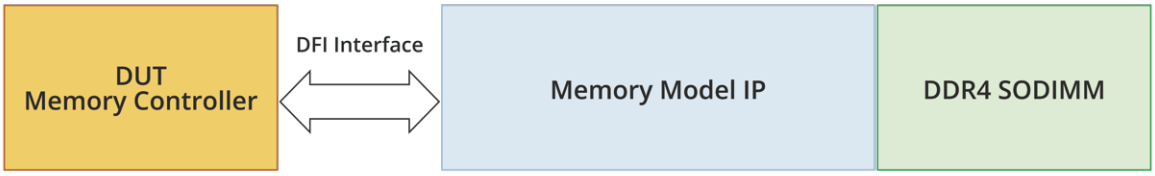
In this approach, HDMI audio and video streams are transmitted directly to a host system. A custom decoder extracts the video and audio data, which are then displayed using a software-based simulation of a monitor.

Similar architectures are applied to DisplayPort, MIPI DSI, and USB speed adaptors. This method allows verification of a monitor. Similar architectures are applied to DisplayPort, MIPI DSI, and USB speed adaptors. This method allows verification of high-speed display and multimedia interfaces, even when the FPGA prototyping cannot operate at the full peripheral speed. It ensures that video and audio pipelines can be tested and analyzed under conditions that reflect actual system behavior.



Case 3: Memory Model

FPGA prototyping systems are often limited in the types of memory they can support directly. To validate DDR5, LPDDR5, and HBM2E/3 memory controllers, memory model IP is used to emulate the behavior of these memories using DDR4 hardware available on the FPGA. For system debugging, S2C's memory model includes a backdoor that provides controllable and observable access to memory reads and writes. This capability allows efficient testing and validation of memory interfaces. It also supports early detection of design issues and verification of system-level functionality.



S2C has built a wide range of speed adaptors, memory models, and over 90 ready-to-use daughter cards to address complex peripheral connectivity challenges. These solutions enable customers to overcome the difficulties associated with connecting high-speed peripherals and unsupported memory to achieve fast deployment.

With more than twenty years of experience in FPGA prototyping, S2C continues to invest in developing and expanding support for additional protocols and interface standards. The company focuses on applying advanced digital EDA technologies in practical prototyping scenarios, helping customers reduce verification cycles and accelerate the time-to-market. By providing reliable speed adaptation and memory modeling solutions, FPGA prototyping can be brought closer to real-world system conditions. This allows engineers to validate designs effectively and efficiently.